

DATA SHEET

74F545

Octal bidirectional transceiver (with
3-State inputs/outputs)

Product specification

1990 Mar 01

IC15 Data Handbook

Octal bidirectional transceiver (with 3-State inputs/outputs)

74F545

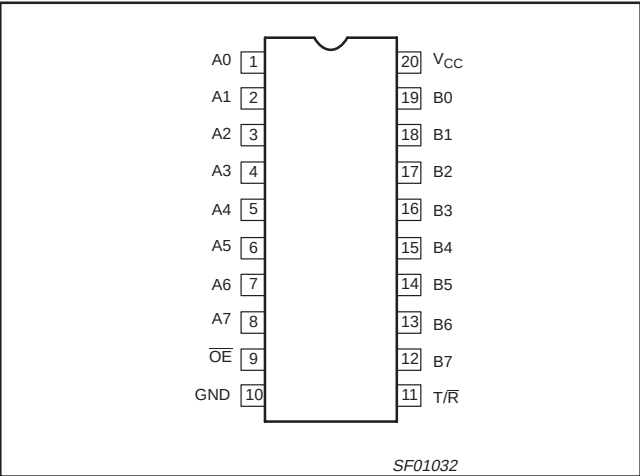
FEATURES

- High impedance NPN base inputs for reduced loading (70µA in High and Low states) output
- 8-bit bidirectional data flow reduces system package count
- 3-State inputs/outputs for interfacing with bus oriented systems
- 24mA and 64mA bus drive capability on A and B ports, respectively
- Transmit/Receive and Output Enable simplify control logic

DESCRIPTION

The 74F545 is an 8-bit, 3-State, high speed transceiver. It provides bidirectional drive for the bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA bus drive capability on the A ports and 64mA bus drive capability on the B ports. One input, Transmit/Receive (T/R) determines the direction of logic signals through the bidirectional transceiver. Transmit enables data from A ports to B ports; Receive enables data from B ports to A ports. The Output Enable input disables both A and B ports by placing them in a 3-State condition. The 74F545 performs the same function as the 74F245, the only difference being package pin assignment.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F545	4.0ns	87mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE V _{CC} = 5V ±10%, T _{amb} = 0°C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F545N	SOT146-1
20-Pin Plastic SOL	N74F545D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

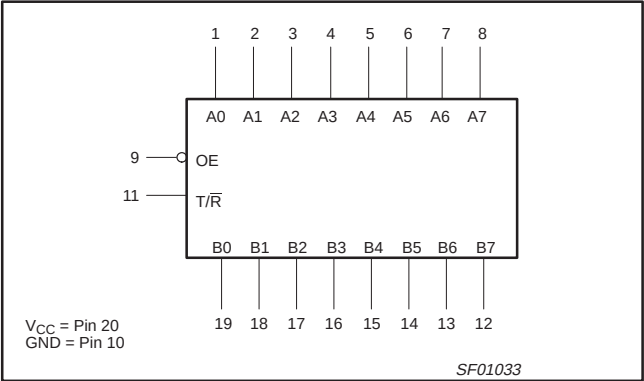
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0–A7, B0–B7	Data inputs	3.5/0.117	70µA/70µA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.067	40µA/40µA
T/R	Transmit/Receive input	2.0/0.067	40µA/40µA
A0 - A7	Port A 3-State outputs	150/40	3.0mA/24mA
B0 - B7	Port B 3-State outputs	750/107	15mA/64mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

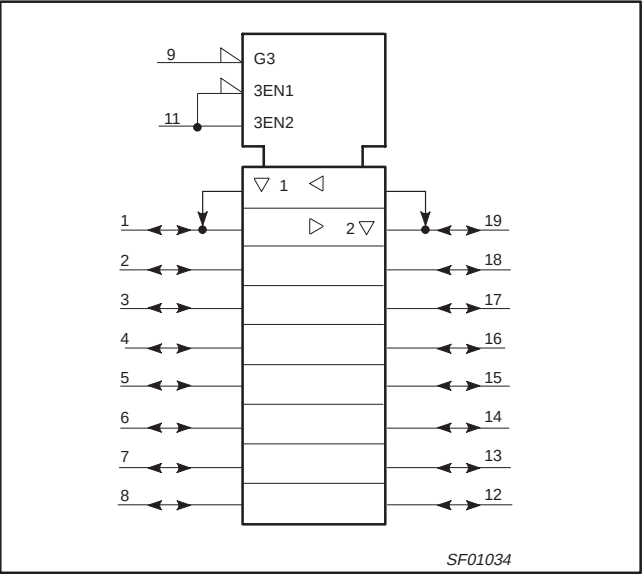
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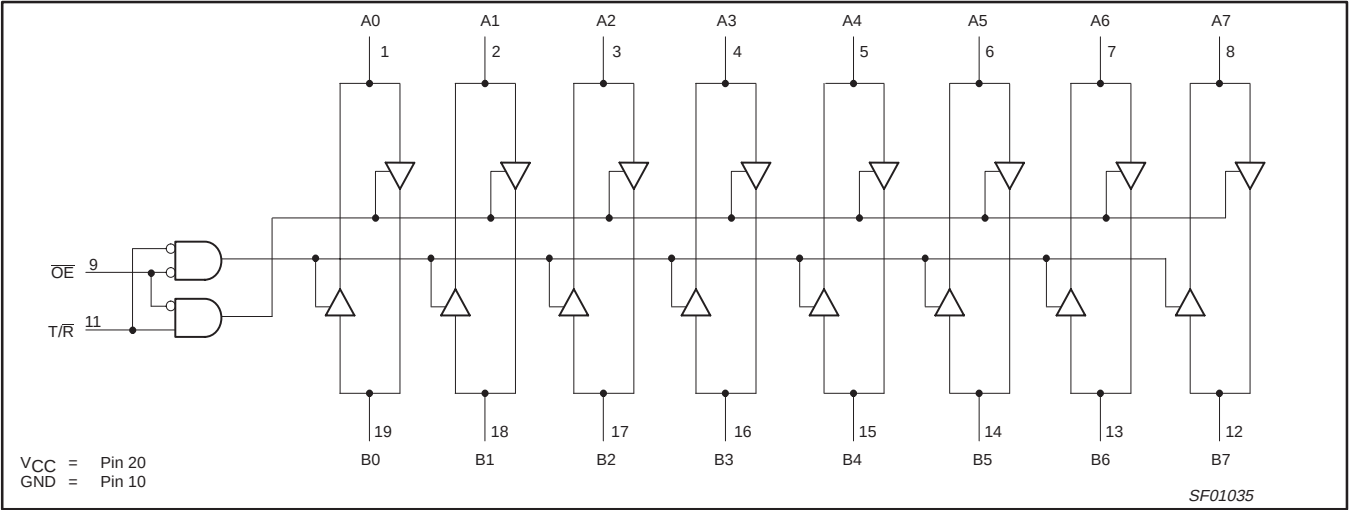
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
OE	T/R	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +5.5	V
I_{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current	A0–A7		−3	mA
		B0–B7		−15	mA
I_{OL}	Low-level output current	A0–A7		24	mA
		B0–B7		64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹			LIMITS			UNIT
						MIN	TYP ²	MAX	
V _{OH}	High-level output voltage	A0–A7 B0–B7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = –3mA	±10%V _{CC}	2.4			V
		±5%V _{CC}			2.7	3.3		V	
		B0–B7		I _{OH} = –15mA	±10%V _{CC}	2.0			V
					±5%V _{CC}	2.0			V
V _{OL}	Low-level output voltage	A0–A7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = 24mA	±10%V _{CC}		0.35	0.50	V
		±5%V _{CC}				0.35	0.50	V	
		B0–B7		I _{OL} = MAX	±10%V _{CC}			0.55	V
					±5%V _{CC}		0.42	0.55	V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				–0.73	–1.2	V
I _I	Input current at maximum input voltage	OE, T/R	V _{CC} = 0.0V, V _I = 7.0V					100	μA
		A0–A7, B0–B7	V _{CC} = 5.5V, V _I = 5.5V					1.0	mA
I _{IH}	High-level input current	OE, T/R only	V _{CC} = MAX, V _I = 2.7V					40	μA
I _{IL}	Low-level input current		V _{CC} = MAX, V _I = 0.5V					–40	μA
I _{OZH} +I _{IH}	Off-state output current High-level voltage applied		V _{CC} = MAX, V _I = 2.7V					70	μA
I _{OZL} +I _{IL}	Off-state output current Low-level voltage applied		V _{CC} = MAX, V _I = 0.5V					–70	μA
I _{OS}	Short-circuit output current ³	A0–A7	V _{CC} = MAX			–60		–150	mA
		B0–B7				–100		–225	μA
I _{CC}	Supply current (total) ⁴	I _{CCH}	V _{CC} = MAX	T/R=A _n =4.5V, OE=GND		84	100	mA	
		I _{CCL}		OE=T/R =B _n =GND		96	120	mA	
		I _{CCZ}		T/R=B _n =GND, OE=4.5V		96	120	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.
- Measure I_{CC} with outputs open.

AC ELECTRICAL CHARACTERISTICS

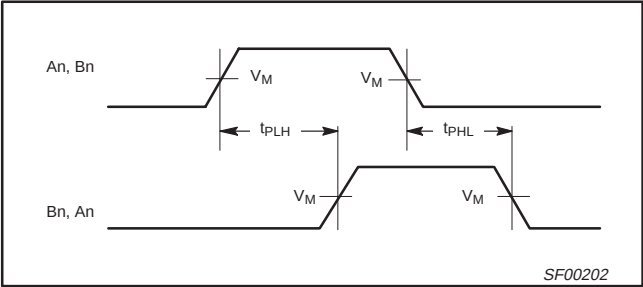
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH}	Propagation delay An to Bn, Bn to An	Waveform 1	1.5	3.5	5.5	1.5	6.5	ns	
t _{PHL}			2.5	4.5	6.5	2.5	7.0	ns	
t _{PZH}	Output Enable time to High or Low level	Waveform 2	6.0	8.5	10.5	6.0	11.0	ns	
t _{PZL}		Waveform 3	5.5	8.0	9.5	5.5	10.0	ns	
t _{PHZ}	Output Disable time from High or Low level	Waveform 2	2.5	5.0	7.0	2.5	8.0	ns	
t _{PLZ}		Waveform 3	2.0	4.5	6.5	2.0	7.5	ns	

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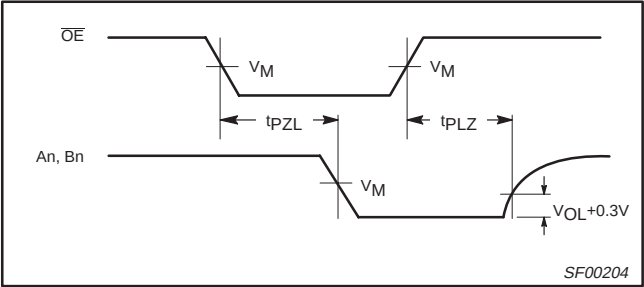
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AC WAVEFORMS

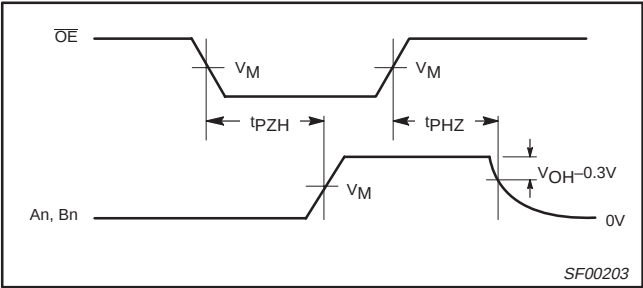
For all waveforms, $V_M = 1.5V$.



Waveform 1. Propagation Delay Data for Non-Inverting Output



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORM

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Definition

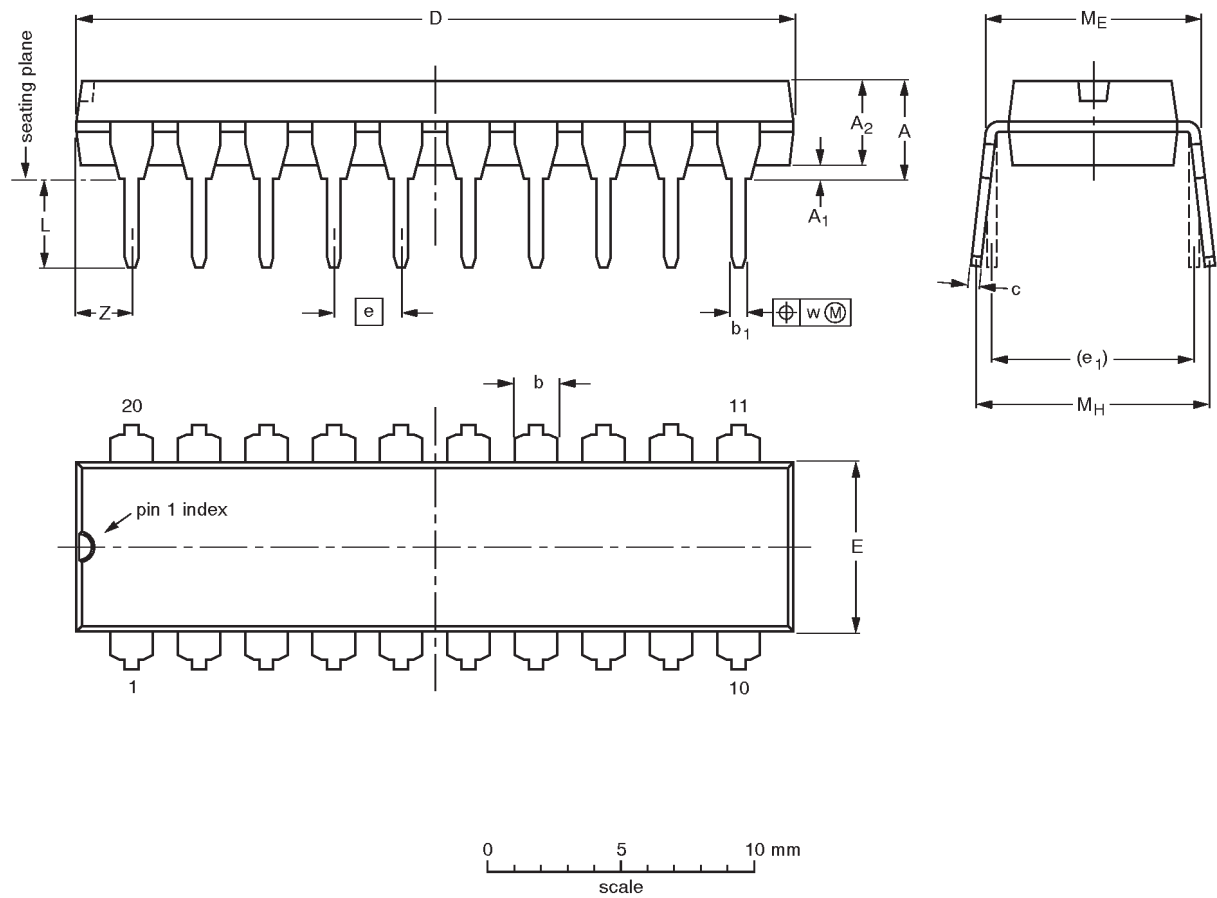
family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

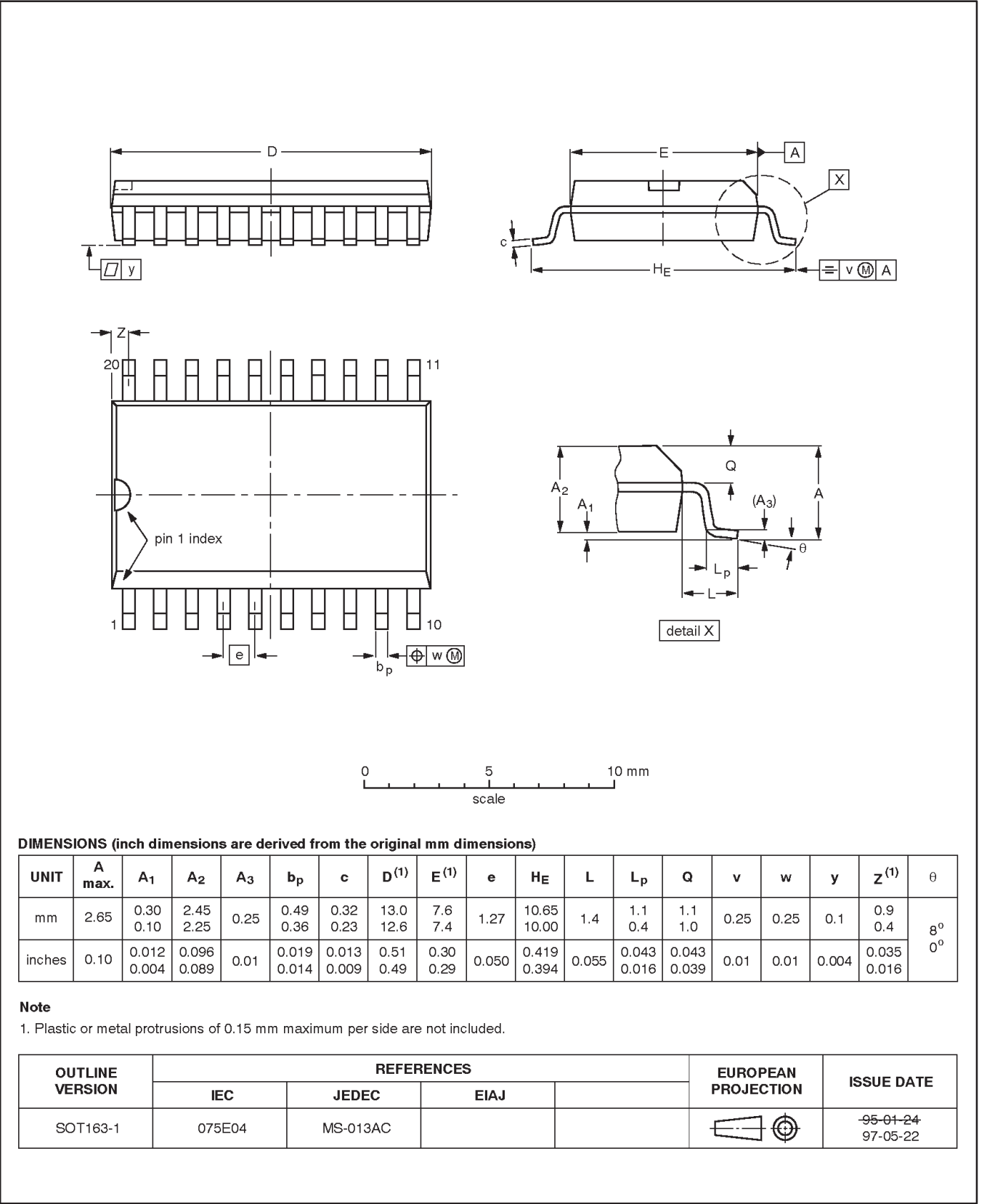
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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NOTES

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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